MHS
MATRA-HARRIS SEMICONDUCTOR

data sheet

HM 65747
4K x 1
HIGH SPEED CMOS SRAM

JANUARY 1987

Features

- HIGH SPEED, FAST ACCESS TIME : 25/35/45 ns
- ASYNCHRONOUS INPUTS
- STAND BY CURRENT : 10 mA max
- OPERATING SUPPLY CURRENT : 80 mA max
- MULTIPLEXED DATA INPUT AND OUTPUT
- NO CLOCKS OR STROBES REQUIRED
- WIDE TEMPERATURE RANGE : – 55° C TO 125° C
- TTL COMPATIBLE INPUTS AND OUTPUTS
- SINGLE 5V SUPPLY
- CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE

Description

The HM 65747 is a 4096 bit static Random Access Memory organized as 4096 words by 1 bit using CMOS technology and operates from the single 5V supply.

The HM 65747 uses MHS technology featuring a very fast access time.

A 25 ns access time is available with a maximum power consumption of 495 mW.

Easy memory expansion is provided by an active low chip select ($\overline{CS}$) and three state drivers.

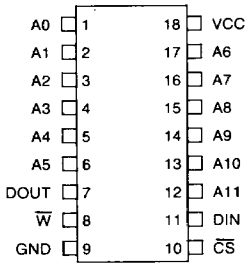
The HM 65747 has an automatic power down feature, reducing the power consumption by 80 %.

This product features fully static operation requiring no external clocks or timing strobes. The pinout is the Jedec 18 pin "300" width package allowing maximum board packing density.

The HM 65747 military RAM is 100 % processed using the STD MIL 883C test methods. This makes an ideally product suited to military temperature application requiring the highest level of performance and reliability.

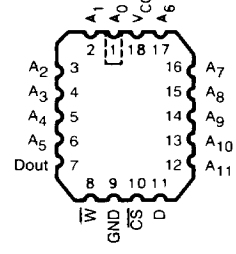
Pinout (TOP VIEWS)

DIP
(18 PINS)

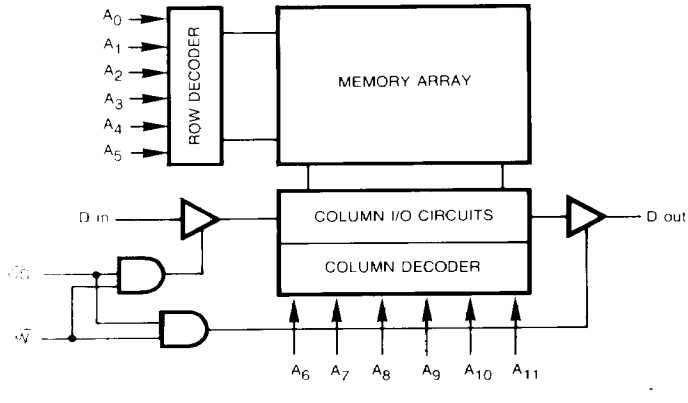


A-Address input
DOUT-Data output
DIN-Data in
$\overline{CS}$-Chip Select
$\overline{W}$-Write enable
VCC-Power
GND-Ground

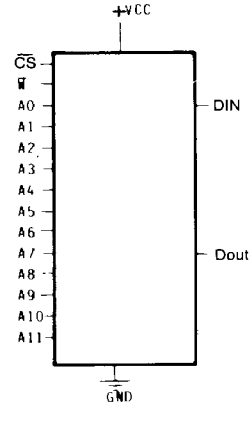
LCC
(18 LEADS)



Functional Diagram



Logic Symbol



87-01-HM 65747/C341

• ABSOLUTE MAXIMUM RATINGS	• OPERATING RANGE		
		Operating Voltage	Operating Temperature
Supply voltage (VCC-GND) — 0.5 V to + 7.0 V			
DC input voltage : − 3.0 to 7.0V DC output voltage in high Z state : − 0.5V to 7.0V Storage temperature : − 65° C to + 150° C Output current into outputs (low) : 20 mA	Military - 2	VCC ± 10 %	− 55° C to + 125° C
	Commercial - 5	VCC ± 10 %	− 0° C to + 70° C

Electro Static Discharge Voltage > 2000V
(per MIL STD 883, Method 3015.2)

ELECTRICAL CHARACTERISTICS

DC PARAMETERS

Symbol	Parameter	65747H-5	65747K-5 65747M-5	65747K-2 65747M-2	Unit	Value
ICCSB (1)	Stand by supply current	15	10	10	mA	max
ICCOP (2)	Average operating supply current	90	80	110	mA	max
IIX (3)	Input leakage current	± 10	± 10	± 10	μA	max
IOZ (3)	Output leakage current	± 50	± 50	± 50	μA	max
VIL (4)	Input low voltage	0.8	0.8	0.8	V	max
VIH (4)	Input high voltage	2.0	2.0	2.0	V	min
VOL (5)	Output low voltage	0.4	0.4	0.4	V	max
VOH (5)	Output high voltage	2.4	2.4	2.4	V	min
I OS (6)	Output short circuit current	− 350	− 350	− 350	mA	max
C IN (7)	Input capacitance	5	5	5	PF	max
C OUT (7)	Output capacitance	6	6	6	PF	max

Note 1 : $\overline{CS} \geqslant VIH$
Note 2 : VCC max, Iout = 0 mA
Note 3 : GND ⩽ VI ⩽ VCC, GND ⩽ VO ⩽ VCC Output disabled
Note 4 : VIL min = − 3.0 V, VIH max = VCC
Note 5 : VCC = min, IOH = − 4 mA, IOL = 12 mA commercial/IOL = 8 mA military
Note 6 : VCC = max, Vout = GND, duration of the short circuit should not exceed 30 seconds
Not more than 1 output should be shorted at one time.
Note 7 : This parameter is sampled and not 100 % tested. TA = 25°C, F = 1 MHz, VCC = 5.0V

AC PARAMETERS

Conditions

Input pulse levels	GND to 3.0 V
Input rise time	5 ns
Input timing reference levels	1.5 V
Output loading IOL/IOH (see fig. 1a and 1b)	+ 30 pF

Read cycle

Parameter	Description	65747H-5	65747K-5	65747K-2	65747M-5	65747M-2	Unit	Value
TAVAV	Read cycle time	25	35	35	45	45	ns	min
TAVQV	Address to data valid	25	35	35	45	45	ns	max
TAVQX	Data hold from address change	3	3	3	3	3	ns	min
TELQV	$\overline{CS}$ low to data valid	25	35	35	45	45	ns	max
TELQX	$\overline{CS}$ low to low Z (9)	5	5	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z (8, 9)	15	20	20	25	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	0	ns	min
TEHICCL	$\overline{CS}$ high to power down	20	25	25	30	30	ns	max

Write cycle (10)

Parameter	Description	65747H-5	65747K-5	65747K-2	65747M-5	65747M-2	Unit	Value
TAVAV	Write cycle time	25	35	35	45	45	ns	min
TELWH	$\overline{CS}$ low to write end	25	35	35	45	45	ns	min
TAVWH	Address set up to write end	25	35	35	45	45	ns	min
TWHAX	Address hold from write end	0	0	0	0	0	ns	min
TAVWL	Address set up to write start	0	0	0	0	0	ns	min
TWLWH	$\overline{W}$ pulse width	15	20	20	25	25	ns	min
TDVWH	Data set up to write end	15	20	20	25	25	ns	min
TWHDX	Data hold from write end	0	10	10	10	10	ns	min
TWLQZ	$\overline{W}$ Low to high Z (9)	15	20	20	25	25	ns	max
TWHQX	$\overline{W}$ high to low Z (8, 9)	0	0	0	0	0	ns	min

Note 8 : TEHQZ, TWLQZ are tested with C1 = 5 pF as in figure 1b. Transition is measured ± 500 mV from steady state voltage.

Note 9 : At any given temperature and voltage contion, TEH/TWH is less than TEL/TWL for all devices. These parameters are sampled and not 100 % sampled.

Note 10 : Data input set up and hold timing should be referenced to the rising edge of the signal that terminates the write.

AC TEST LOADS AND WAVEFORMS

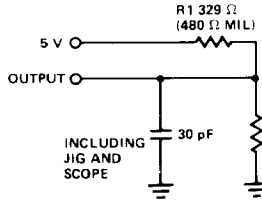


Figure 1a

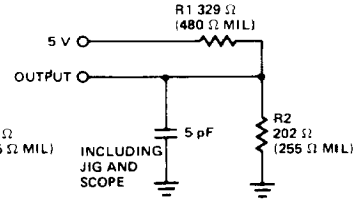


Figure 1b

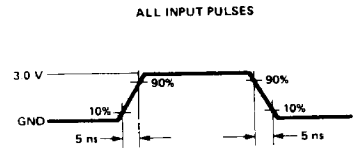


Figure 2

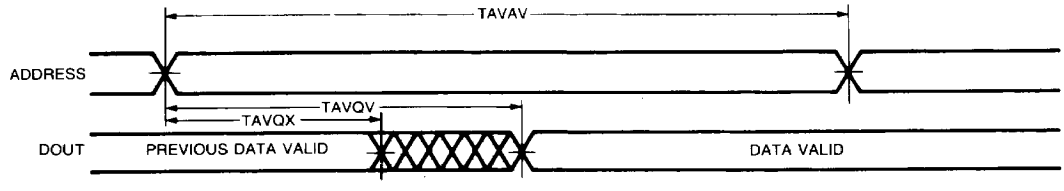
TRUTH TABLE

$\overline{CS}$	$\overline{W}$	DIN	DOUT	MODE
H	X	Z	Z	DESELECT
L	H	Z	VALID	READ
L	L	VALID	Z	WRITE

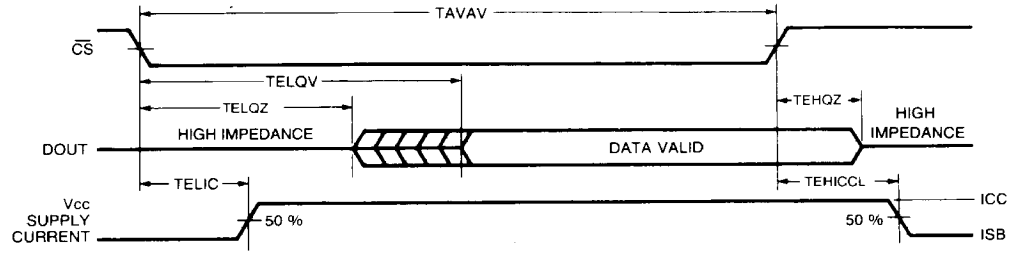
X : "H" or "L"

SWITCHING WAVEFORMS

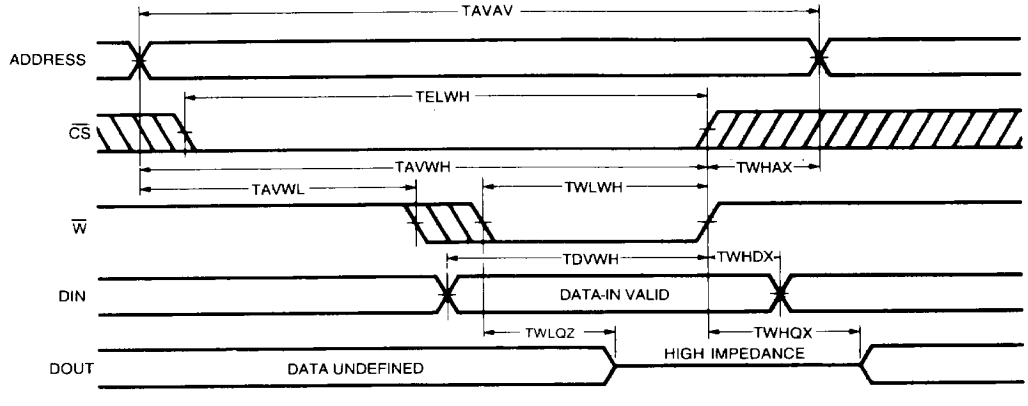
READ CYCLE No. 1 (Notes 11, 12)



READ CYCLE No. 2 (Notes 11, 13)

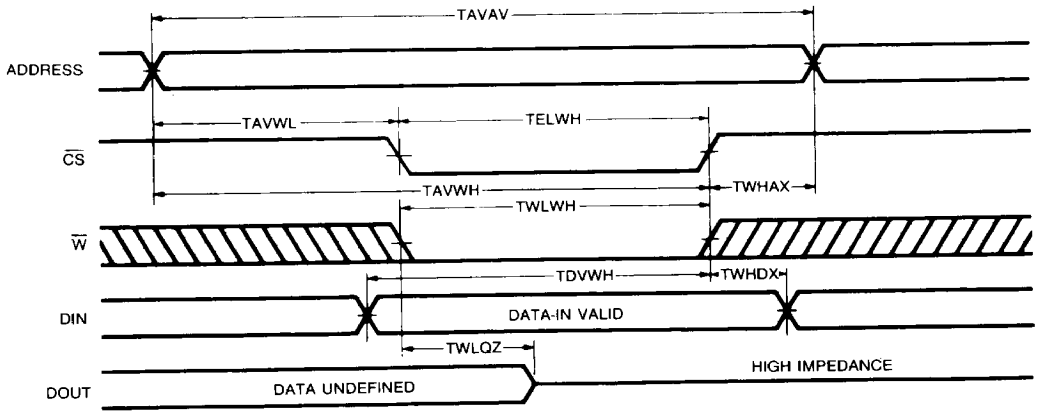


WRITE CYCLE No. 1 ($\overline{W}$ Controlled)



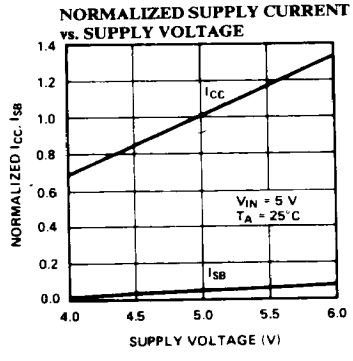
Note 11 : $\overline{W}$ is high for read cycle
Note 12 : Device is continuously selected $\overline{CS}$ = VIL
Note 13 : Address valid prior to or concident with $\overline{CS}$ transition low

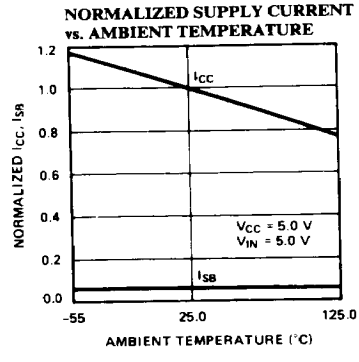
WRITE CYCLE No. 2 ($\overline{CS}$ Controlled)

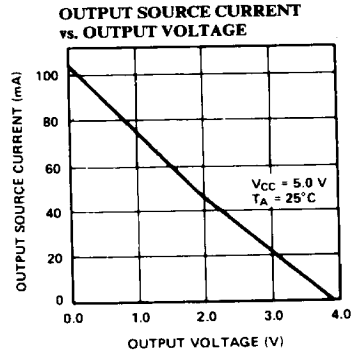


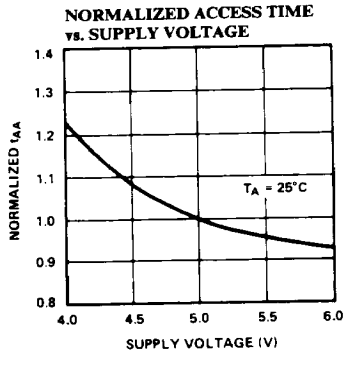
Note : If $\overline{CS}$ goes high simultaneously with $\overline{W}$ high, the output remains in a high impedance state.

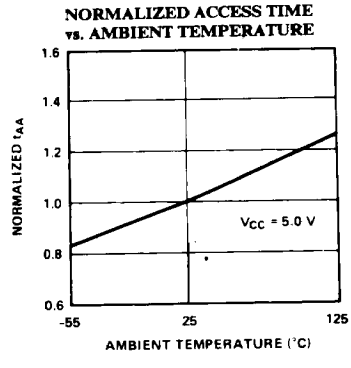
TYPICAL DC AND AC CHARACTERISTICS

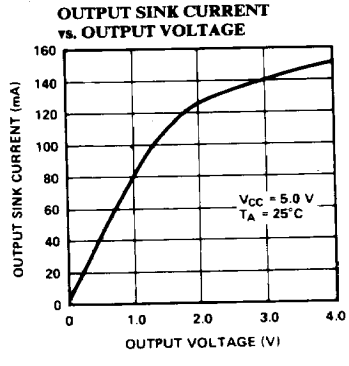


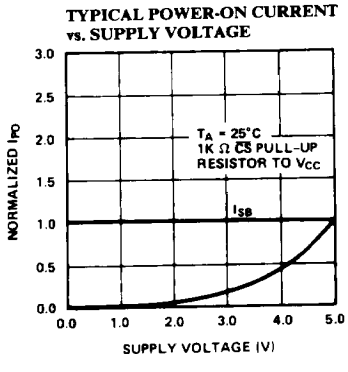


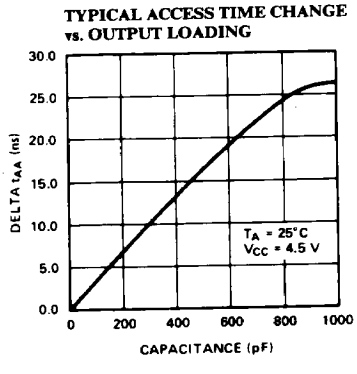


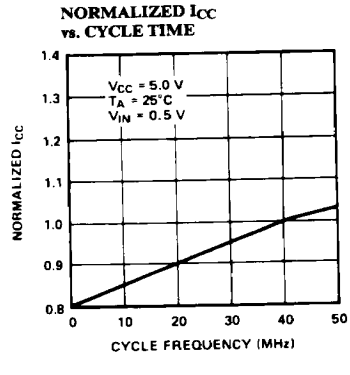






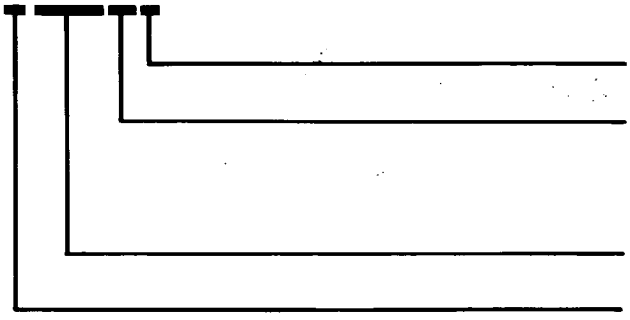






Ordering information

DEVICE TYPE	PACKAGE	TEMPERATURE RANGE
HM1-65747( )-5	CERAMIC DIL	0°C to + 70°C
HM1-65747( )-2	CERAMIC DIL	– 55°C to + 125°C
HM1-65747( )-8	CERAMIC DIL	– 55°C to + 125°C
HM3-65747( )-5	PLASTIC DIL	0°C to + 70°c
HMT-65747( )-5	SO PLASTIC DIL	0°C to + 70°C
HM4-65747( )-5	LCC 18 PIN	0°C to + 70°C
HM4-65747( )-2	LCC 18 PIN	– 55°C to + 125°C
HM4-65747( )-8	LCC 18 PIN	– 55°C to + 125°C



TEMPERATURE RANGE (– 2, – 5, – 8)

PERFORMANCE :
H : 25 ns (commercial only)
K : 35 ns
M : 45 ns

DEVICE TITLE

PACKAGE (1, 3, 4)
1 : CERAMIC
3 : PLASTIC
4 : LCC
T : SO

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Fax (33) 1-30640693

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